UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/828,283	04/05/2001	Kenneth J. Mobley	RAM 465	6330

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William J. KUBIDA, Esq.
Hogan & Hartson, LLP
1200 17th Street, Suite 1500
Denver, CO 80202

EXAMINER
KIM, HONG CHONG

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/04/2003   *5*

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

	Application No.		**Applicant(s)**	
Office Action Summary	09/828,283		MOBLEY, KENNETH J.	
	Examiner		**Art Unit**	
	Hong C Kim		2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *05 April 2001* .

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-24* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-24* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *4/5/01* is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

1.   Claims 1-24 are presented for examination. This office action is in response to the

amendment filed on 4/5/01.

2.   Receipt is acknowledged of information disclosure statement filed on 7/9/01, which the

statement has been placed of record in the file. Information disclosed and listed on PTO 1449

was considered.

Claim Objections

3.   Claims 1-20 are objected to because of the following informalities: A broad term

"substantially" should be deleted in the claims. The term "substantially" is often used in

conjunction with another term to describe a particular characteristic of the claimed invention. It is

a broad term. In re Nehrenberg, 280 F.2d 161, 126 USPQ 383 (CCPA 1960). The court held that

the limitation "to substantially increase the efficiency of the compound as a copper extractant"

was definite in view of the general guidelines contained in the specification. In re Mattison, 509

F.2d 563, 184 USPQ 484 (CCPA 1975). The court held that the limitation "which produces

substantially equal E and H plane illumination patterns" was definite because one of

ordinary skill in the art would know what was meant by "substantially equal." Andrew

Corp. v. Gabriel Electronics, 847 F.2d 819, 6 USPQ2d 2010 (Fed. Cir. 1988).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.   Claims 17-24 are rejected under 35 U.S.C. 102(b) as being anticipated by *Leung et al.,*

(Leung) U.S. Patent 5,394,534 or *Alwais et al. (Alwais)* U.S. Patent 5,991,851.

As to claim 17 , Leung discloses the invention as claimed. Leung discloses a memory

in a memory device (Fig. 1) having a non-array row external (Fig. 1 Refs. 185 and 187) to plural

DRAM sub-arrays (Fig. 1 Refs. 0-63), for receiving from the DRAM sub-array referenced by an

address of an access request, the improvement comprising: a command decoder (Fig. 1 Refs.

182, 183, and 195 and col. 10 line 37 thru col. 11 lin 35) for internally determining when a

refresh cycle can be hidden behind an access to the non-array row; and a controller (Fig. 1 Ref.

195 and col. 10 line 37 thru col. 11 lin 35) for limiting refresh cycles to a subset of possible times

internally determined by the command decoder.

As to claim 22, Leung discloses the invention as claimed above. Leung further discloses

the non-array row comprises an SRAM row (Fig. 1 Refs. 185 and 187).

As to claim 23, Leung discloses the invention as claimed above.   Leung further discloses

the controller comprises a missed refresh counter for tracking a number of refreshes missed by at

least one of the plural DRAM sub-arrays (col. 3).

As to claim 24, Leung discloses the invention as claimed above.   Leung further discloses

the controller further comprises a refresh counter for storing a next array row to be refreshed in at

least one of the plural DRAM sub-arrays (Fig.3 Ref. 208).

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Alternatively, As to claim 17, Alwais discloses the invention as claimed. Alwais discloses a

memory in a memory device (Fig. 1) having a non-array row external (Fig. 1 Ref. 14) to plural

DRAM sub-arrays (Fig. 1 Ref. 12), for receiving from the DRAM sub-array referenced by an

address of an access request, the improvement comprising: a command decoder (Fig. 1 Ref. 18

and col. 9 lines 1-3) for internally determining when a refresh cycle can be hidden behind an

access to the non-array row; and a controller (Fig. 1 Ref. 28) for limiting refresh cycles to a

subset of possible times internally determined by the command decoder.

As to claim 22, Alwais discloses the invention as claimed above.   Alwais further

discloses the non-array row comprises an SRAM row (Fig. 1 Ref. 14).

As to claim 23, Alwais discloses the invention as claimed above. Alwais further

discloses the controller comprises a missed refresh counter for tracking a number of refreshes

missed by at least one of the plural DRAM sub-arrays (Fig. 6).

As to claim 23, Alwais discloses the invention as claimed above. Alwais further

discloses the controller further comprises a refresh counter for storing a next array row to be

refreshed in at least one of the plural DRAM sub-arrays (Fig.6).

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

7.   Claims 1-20 are rejected under 35 USC § 103(a) as being unpatentable over *Alwais et al.*

(Alwais) U.S. Patent 5,991,851 in view of *Leung et al., (Leung)* U.S. Patent 5,394,534.

As to claim 1, *Alwais*, discloses In a memory device having plural DRAM sub-arrays (fig.

3 Ref 12), each with plural array rows, the improvement comprising: an address decoder for

decoding an address of a memory access request and indicating which of the plural DRAM sub-

arrays are referenced by the memory access request (Fig. 1 Ref. 18); and refresh circuitry,

responsive to the indication of the address decoder (Fig. 1 Ref. 28), however, Alwais does not

specifically disclose the refresh circuitry to refresh at least one array row of at least one of the

plural DRAM sub-arrays not referenced by the memory access request while substantially

contemporaneously performing the memory access request.

Leung discloses the refresh circuitry to refresh at least one array row of at least one of the

plural DRAM sub-arrays not referenced by the memory access request while substantially

contemporaneously performing the memory access request (abstract lines 9-10) for the purpose

of increasing access speed by preventing interference between refreshing of memory cells and

accessing the memory cells externally. It is desirable in the memory art to increase access speed

because it would allow to increase bandwidth and increase the system performance.

Therefore, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to incorporate the refresh circuitry to refresh at least one array row of at

least one of the plural DRAM sub-arrays not referenced by the memory access request while

substantially contemporaneously performing the memory access request as taught by Leung into

Alwais for the advantages stated above.

As to claim 2, Alwais and Leung disclose the invention as claimed above. Leung further

discloses the memory access request comprises a read access request (abstract lines 9-10).

As to claim 3, Alwais and Leung disclose the invention as claimed above. Leung further

discloses comprising a non-array row, external to the plural DRAM sub-arrays, for receiving

from the DRAM sub-array referenced by the address of the read access request at least a portion

of an array row corresponding to the address of the read access request (Fig. 1 Ref. 187).

As to claim 4, Alwais and Leung disclose the invention as claimed above. Leung further

discloses the non-array row comprises an SRAM row (Fig. 1 Ref. 187).

As to claim 5, Alwais and Leung disclose the invention as claimed above. Alwais further

discloses a tag register (col. 4 line 41, cache reads on this limitation since a cache stores an

address (tag) and data in cache memory) for storing at least a portion of the address of a read

access request that last stored information into the non-array row; and a command decoder (col.

4 lines 47-61) for signaling that the read access request may be serviced from the non-array row

rather than the array row corresponding to the address of the read access request.

As to claim 6, Alwais and Leung disclose the invention as claimed above. Leung further

discloses the memory access request comprises a write access request (abstract lines 9-10).

As to claim 7, Alwais and Leung disclose the invention as claimed above. Leung further

discloses a non-array row, external to the plural DRAM sub-arrays, for storing (Fig. 1 Refs 185

and 187), prior to writing to the DRAM sub-array referenced by the address of the write access

request, at least a portion of an array row corresponding to the address of the write access

request.

As to claim 8, Alwais and Leung disclose the invention as claimed above. Alwais further

discloses the refresh circuitry further comprises a refresh timer for limiting a frequency of

refreshes performed (Fig. 6).

As to claim 9, Alwais and Leung disclose the invention as claimed above. Leung further

discloses the refresh circuitry further comprises a missed refresh counter for tracking a number of

refreshes missed by at least one of the plural DRAM sub-arrays (col. 10 line 35 thru col. 11 line

35).

As to claim 10, Alwais and Leung disclose the invention as claimed above. Alwais

further discloses the refresh circuitry (Fig. 6 Ref. 106) further comprises a refresh counter for

storing a next array row to be refreshed in at least one of the plural DRAM sub-arrays .

As to claim 11, *Alwais* discloses a method of refreshing a memory device having plural

DRAM sub-arrays (Fig. 1 Ref. 12), each with plural array rows , the method comprising: (a)

decoding an address of a memory access request (Fig. 1 Ref. 18); (b) indicating which of the

plural DRAM sub-arrays are referenced by the memory access request (Fig. 1 Ref. 18); and (c)

refreshing (col. 8 line 65 thru col. 9 line 12), in response to the indicating step, at least one array

row of at least one of the plural DRAM sub-arrays not referenced by the memory access request

(Fig. 1 Ref. 28), however, Alwais does not specifically disclose the step of executing the memory

access request, wherein steps (c) and (d) are performed substantially contemporaneously.

Leung discloses executing the memory access request, wherein steps (c) and (d) are

performed substantially contemporaneously (abstract lines 9-10) for the purpose of increasing

access speed by preventing interference between refreshing of memory cells and accessing the

memory cells externally. It is desirable in the memory art to increase access speed because it

would allow to increase bandwidth and increase the system performance.

Therefore, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to incorporate executing the memory access request, wherein steps (c)

and (d) are performed substantially contemporaneously as taught by Leung into Alwais for the

advantages stated above.

As to claim 12, Alwais and Leung disclose the invention as claimed above. Leung further

discloses the memory access request comprises a read access request (abstract lines 9-10).

As to claim 13, Alwais and Leung disclose the invention as claimed above. Leung further

discloses receiving, into a non-array row (fig. 1 refs. 185 and 187) external to the plural DRAM

sub-arrays and from the DRAM sub-array referenced by the address of the read access request, at

least a portion of an array row corresponding to the address of the read access request.

As to claim 14, Alwais and Leung disclose the invention as claimed above. Leung further

discloses the step of receiving comprises receiving the portion into an SRAM row (Fig. 1 Refs.

185 and 187).

As to claim 15, Alwais and Leung disclose the invention as claimed above. Alwais

further discloses storing in a tag register (col. 4 line 41, cache reads on this limitation since a

cache stores an address (tag) and data in cache memory) at least a portion of the address of a read

access request that last stored information into the non-array row; and comparing (col. 4 lines

47-61) whether the read access request may be serviced from the non-array row rather than the

array row corresponding to the address of the read access request.

As to claim 16, Alwais and Leung disclose the invention as claimed above. Leung further

discloses the memory access request comprises a write access request (abstract lines 9-10).

As to claim 17, Alwais and Leung disclose the invention as claimed above. Leung further

discloses storing into a non-array row (Fig. 1 Refs 185 and 187), external to the plural DRAM

sub-arrays, prior to writing to the DRAM sub-array referenced by the address of the write access

request, at least a portion of an array row corresponding to the address of the write access

request.

As to claim 18, Alwais and Leung disclose the invention as claimed above. Alwais

further discloses the refresh circuitry further comprises limiting a frequency of refreshes

performed based on a refresh timer (Fig. 6).

As to claim 19, Alwais and Leung disclose the invention as claimed above. Leung further

discloses tracking a number of refreshes missed by at least one of the plural DRAM sub-arrays

(col. 10 line 35 thru col. 11 line 35).

As to claim 20, Alwais and Leung disclose the invention as claimed above. Alwais

further discloses updating a refresh counter to store a next array row to be refreshed in at least

one of the plural DRAM sub-arrays (Fig. 6).

Conclusion

8.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.   See attached PTO-892.

9.   A shortened statutory period for response to this action is set to expire 3 (three) months

and 0 (zero) days from the mail date of this letter. Failure to respond within the period for

response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02,

710.02(b)).

10.   Applicants are requested to number each line of each <u>claim</u> starting with line number one

to provide easier communication in the future.

11.   When responding to the office action, Applicant is advised to clearly point out the

patentable novelty which he or she thinks the claims present in view of the state of the art

disclosed by the references cited or the objections made. He or she must also show how the

amendments avoid such references or objections.   See 37 C.F.R. § 1.111(c).

12.   When responding to the office action, Applicants are advised to provide the examiner

with the line numbers and page numbers in the application and/or references cited to assist

examiner to locate the appropriate paragraphs.

13.   Any inquiry concerning this communication or earlier communications from the

Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The

Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

    If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's

supervisor, Matt Kim, can be reached on (703) 305-3821.

    Any inquiry of a general nature or relating to the status of this application should be

directed to the Group receptionist whose telephone number is (703) 305-3900.

14.   **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
After-Final   (703) 746-7238
Official   (703) 746-7239 (for formal communications intended for

entry)

Non-Official/Draft (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
August 28, 2003